GF40: RF

Libraries

Name	Process	Form Factor
RGO_GF40_25V33_LP_20C_RF	LP	Staggered CUP

Summary

The RF library provides Analog / RF I/O cells including LNA input pads, a 5V tolerant PA output pad and a 10GHz analog signal pad with multiple input resistance options. Discrete components (RF diodes and SCR's) are provided to enable construction of a custom ESD protection solution.

This 40nm library is available in a staggered CUP wire bond implementation with a flip chip option.

ESD Protection:

- JEDEC compliant
  - 2kV ESD Human Body Model (HBM)
  - 200V ESD Machine Model (MM)
  - 500V ESD Charge Device Model (CDM)

Latch-up Immunity:

- JEDEC compliant
  - Tested to I-Test criteria of ± 100mA @ 125°C

RF Diodes

A set of PPLUS_NWELL_DIODE RF diodes provide minimum capacitance for RF applications and high current handling capability for good ESD protection.

Silicon-Controlled Rectifiers (SCR)

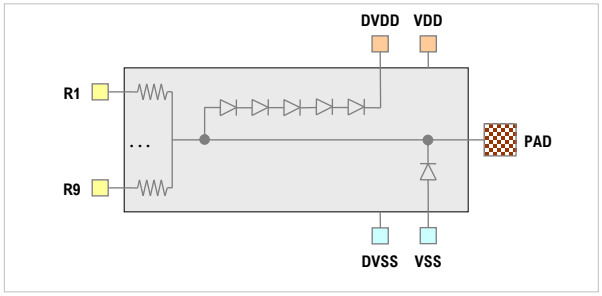
A set of P+ to Nwell SCR discrete components provide the lowest capacitance with the highest ESD protection. These components have been used in I/O pads to demonstrate over 6KV ESD protection.

ANP_BI_DWR_5T

ANP_BI_DWR_5T is a 10 GHz bi-directional analog (thick gate) signal pad with selectable input resistance. Resistors R1 to R4 and R6 to R9 can be used in parallel to achieve the desired resistance value as low as 1.3 ohms.

This structure can then be used with output amplifiers for which R5 can be used in the feedback path. If used in this manner, R1 to R4 and R6 to R9 should be individually connected to isolated fingers of the driver transistors.

The stacked diode ESD structure from DVDD to the I/O pin provides extended overvoltage protection.

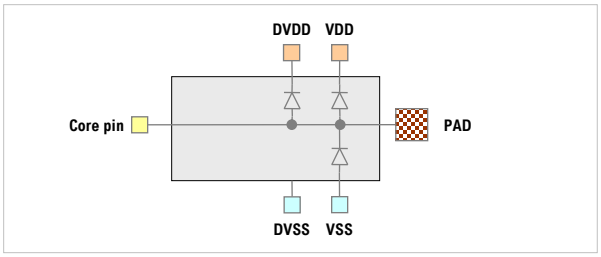


PAD capacitance: 1.487 pF

Analog / RF Pads

ANP_IN_LNA_10V

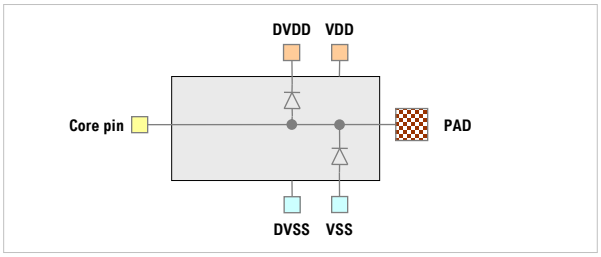
ANP_IN_LNA_10V is a 0 to 1.1V analog I/O pad optimized for low capacitance and designed to protect thin gate oxide input devices.



PAD capacitance: 1.878 pF

ANP_IN_LNA_33V

ANP_IN_LNA_33V is a 0 to 3.3V analog I/O pad optimized for low capacitance.

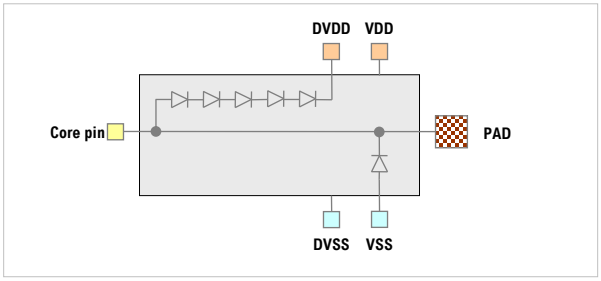


PAD capacitance: 1.445 pF

ANP_OU_PWA_5T

ANP_OU_PWA_5T is an analog I/O pad optimized for low capacitance which uses SCRs for ESD clamp devices.

The stacked diode ESD structure from DVDD to the I/O pin provides extended overvoltage protection. With a 3.3V power supply, this I/O pad is 5V tolerant. Dropping to an I/O domain power supply of 1.8V, the pad is 3.3V tolerant.



PAD capacitance: 1.470 pF

Recommended operating conditions

	Description	Min	Nom	Max	Units
V_{VDD}	Core supply voltage	0.90	1.0	1.10	V
		0.99	1.1	1.21	V
		1.08	1.2	1.26	V
V_{DVDD}	I/O supply voltage	2.97	3.3	3.63	V
		2.70	3.0	3.30	V
		2.52	2.8	3.08	V
		2.25	2.5	2.75	V
		1.62	1.8	1.98	V
T_J	Junction temperature	-40	25	175	°C
V_{PAD}	Voltage at PAD	V_{DVSS} -0.3	-	V_{DVDD} +0.3	V

Cell Size & Form Factor

Staggered Cells	Width	Height	Units
ANP_IN_LNA_10V	25	180	µm
ANP_IN_LNA_33V	25	180	µm
ANP_OU_PWA_5T	25	180	µm
ANP_BI_DWR_5T	25	180	µm
Discrete Components	**Width**	**Height**	**Units**
PPLUS_NWELL_DIODE_S	19	1.93	µm
PPLUS_NWELL_DIODE_M	19	3.53	µm
PPLUS_NWELL_DIODE_L	21.8	6.9	µm
PPLUS_NWELL_DIODE_V	21.8	13.3	µm
RF_SCR20_NO_STI	10	10.1	µm
RF_SCR40_NO_STI	20	10.1	µm

Characterization Corners

Nominal VDD	Model	VDD	DVDD[1]	Temperature
1.2	FF	+5%	+10%	-40°C
	FFF	+5%	+10%	125°C
	FFF	+5%	+10%	150°C
	FFF	+5%	+10%	175°C
	TT	nominal	nominal	25°C
	SS	-10%	-10%	-40°C
	SS	-10%	-10%	125°C
	SS	-10%	-10%	150°C
	SS	-10%	-10%	175°C
1.1 / 1.0	FF	+10%	+10%	-40°C
	FFF	+10%	+10%	125°C
	FFF	+10%	+10%	150°C
	FFF	+10%	+10%	175°C
	TT	nominal	nominal	25°C
	SS	-10%	-10%	-40°C
	SS	-10%	-10%	125°C
	SS	-10%	-10%	150°C
	SS	-10%	-10%	175°C

[1] DVDD = 1.8, 2.5, 2.8, 3.0 and 3.3V